Study and application of the DC self-heating effect estimation method in FinFETs

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***Abstract*— In this paper, the recently proposed DC method for estimating the self-heating effect is studied and reviewed, and, to further test the algorithm, it is applied to different FinFET devices. It was observed experimentally that, for shorter channel lengths, the thermal resistance is larger, which means a higher self-heating effect over the device if operating under the same power conditions.**

Keywords—self-heating effect; FinFET; Silicon-On-Insulator (SOI)

I. INTRODUCTION

Due to the ever-smaller transistor's dimensions and the use of new materials with low thermal conductivity, the performance of advanced technologies is affected by the self-heating effect (SHE) [1], becoming a concern to the microelectronics industry in recent years. Devices under the effects of self-heating suffer a temperature increase, causing mobility reduction, compromising reliability and generating signal delays, influencing the efficiency of analogic circuits, and affecting the performance of digital circuits [2].

Recently, a new method has been proposed to characterize this effect through DC curves [3], which makes it simpler and more accessible, since the required measurements can be obtained without the use of equipment that operates in radiofrequencies, thus justifying a study of this method.

The Silicon-On-Insulator (SOI) transistor, schematically represented in Fig. 1, has an extra insulation oxide beneath the channel, also known as buried oxide [4]. These have favorable electrical characteristics in many aspects, such as the smaller junction capacitance and the reduction of the short channel effects, enabling the further reduction of the devices' dimensions into the submicron scale [4]; however, they become more susceptible to the SHE because its buried oxide acts as a thermal insulator, worsening the heat dissipation from the channel. Nevertheless, its electrical advantages greatly surpass its thermal shortcomings, allowing it to be widely present in today's market.

The Fin Field Effect Transistor, also known as FinFET, is a type of non-planar transistor used in modern processors and other high-end applications. This technology was introduced as a result of the continuous efforts to reduce the size of the transistors [2], aiming to increase the performance of the devices and to overcome some of the problems presented by the planar SOI transistors when entering the nanometric scale, such as the short channel effect.

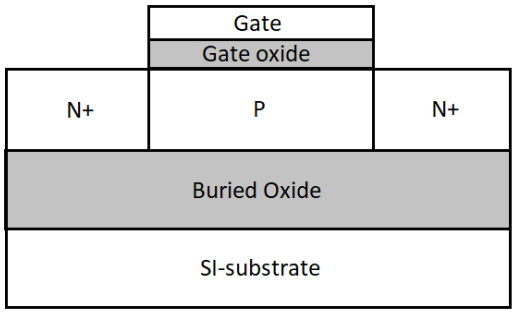

Fig. 1. The SOI MOSFET

Devices based on FinFET technology have a conducting channel raised above the insulator, creating a thin silicon structure in the form of a fin, around which the gate electrode is built. This construction results in a better electrostatic coupling of the device, which allows a better control of charges in the channel, meaning that the short channel effects can be avoided for even smaller channel lengths.

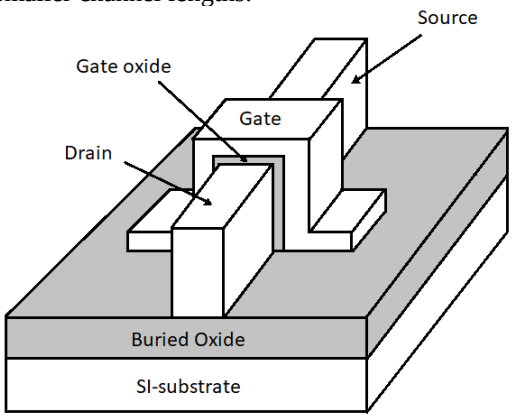

Fig. 2. The FinFET in perspective.

II. DC SELF HEATING METHOD

A. *Causes of the self-heating effect*

The drain current (I_D) in saturation of a FinFET transistor can be represented as shown in equation (1).

$$I_D = \mu_{eff} C_{ox} (W/L)(V_{GS}-V_t)^2(1+\lambda V_{DS})/2n \quad (1)$$

where C_{ox} is the oxide capacitance, μ_{eff} represents the effective mobility in the channel, W and L are the width and length of the channel respectively, V_{GS} is the voltage applied between the gate and the source, V_t is the threshold voltage, V_{DS} is the voltage applied between the drain and the source, λ represents the modulation factor of the channel and n is the body factor.

The μ_{eff} parameter as a function of the temperature is given by (2):

$$\mu_{eff} = \mu_{eff0}(T/T_0)^{-c} \quad (2)$$

where μ_{eff0} is the effective mobility measured at the temperature T_0 (which is usually room temperature), and the c-factor is the temperature mobility degradation coefficient, which is a mathematical adjustment parameter for this model, bearing no direct physical meaning.

The effect caused by SHE is directly related to the Joule effect. A simplified interpretation for this effect is that, once the current flows through the channel, the collisions of the electrons with the atoms of the conductor transfer momentum to these atoms, increasing their kinetic energy, and, therefore, increasing the lattice temperature. This increase results in a reduction of μ_{eff}, as modeled in (2), which in turn decreases the drain current, as seen in (1).

B. R_{TH} extraction algorithm

Considering the algorithm proposed in [3], two main parameters are defined to represent the thermal effects taking place inside the device: the thermal resistance R_{TH} and the c-factor. Both will be extracted from I_D x V_{DS} curves at room temperature and I_D x V_{GS} at increasing temperatures, where R_{TH} is traditionally the main parameter related to the SHE [1].

Initially, the extraction of V_t is performed using the square root of I_D versus V_{GS} curves. The linear region of each curve obtained at a different external temperature (T_{EXT}) is extrapolated to obtain an intersection with the X-axis (that is, the point where $I_D^{0.5} = 0$ A). The value of V_{GS} at this intersection will be the V_t at T_{EXT}. Once V_t is obtained, the next step is the estimation of the c-factor. For this, the transconductance g_m is obtained for different T_{EXT} at constant and preferably high values of overdrive voltage ($V_{GT} = V_{GS} - V_t$). Hence, V_{GS} must be corrected for each different temperature to obtain a constant V_{GT}, given the dependence of V_t with the temperature.

These g_m values and their respective temperatures are applied in (3), where g_{m0} is the transconductance measured at $T_0 = 300$ K with T varying from 310 K to 400 K, obtaining a first value of the c-factor as a function of temperature, then entering a recursive process that seeks to improve the results of R_{TH} and c-factor. This equation can be derived from (2), if one assumes that g_m is directly proportional to μ_{eff}.

$$c = \frac{\log(g_m) - \log(g_{m,0})}{\log(To) - \log(T)} \quad (3)$$

Then, we obtain the curve of the inverse transistor efficiency (I_D/g_m) as a function of the power applied (P). In (4), a linear approximation obtained from the Taylor series is presented for I_D/g_m in the saturation region, as it was deduced in [3].

$$\frac{I_D}{g_m}(P) \approx M\left(1 + \frac{c.T_{EXT}.R_{TH}.P}{(R_{TH}.P_0 + T_O)^2}\right) \quad (4)$$

Since for low values of P this approximation is not valid, to extract the constant M, a numerical extrapolation of the linear regions of these curves is performed, since $M = I_D/g_m(P = 0)$. With that information, (4) can be used to calculate R_{TH}, where P_0 is a power point to be chosen within the total range, in order to minimize errors, and the recommendation from [3] is to use an average value.

The last step of the recursive process is to update the values of T using (5). This in turn allows during the next iteration a better approximation of the c-factor in (3), resulting in a new R_{TH} value in (4).

$$T = R_{TH}.P + T_{EXT} \quad (5)$$

From this point, if the relative difference of R_{TH} between the current and the previous iterations is less than a pre-established maximal desired error (10^{-5} in this case), the recursive process is terminated, providing an approximation of the values of R_{TH} and the c-factor. Otherwise, the process will recalculate the c-factor, repeating itself until this condition is satisfied, or, in case of numerical divergence, an additional stop condition after one hundred iterations is imposed.

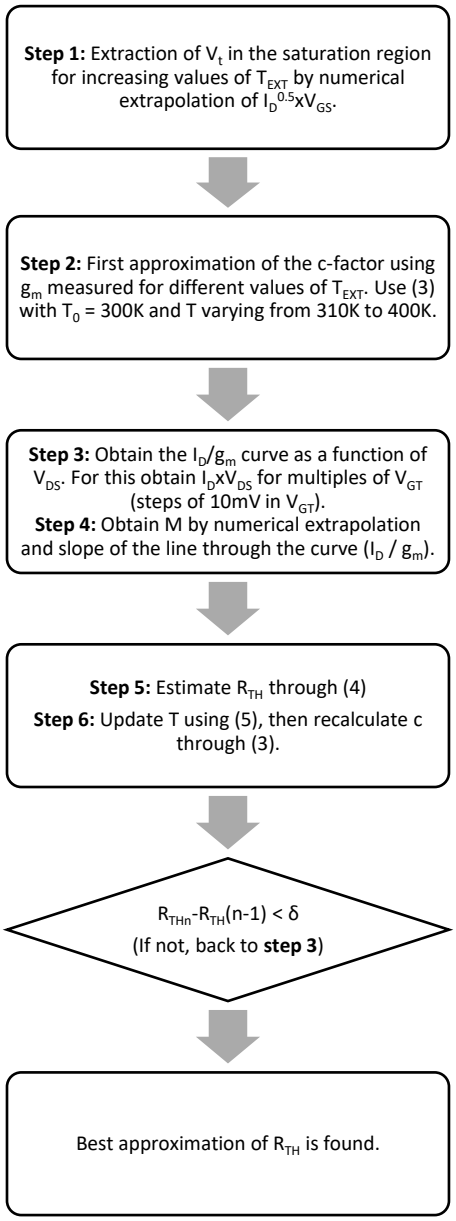

Fig. 3. Flow chart of the thermal resistance estimation algorithm.

III. Devices Characteristics

The devices used in this work were manufactured at IMEC, Belgium, and consist of triple-port MuGFETs doped channel transistors ($N_A = 10^{15}$ cm^{-3}). Its dimensions are fin height (h_{FIN}) of 65nm, gate oxide composed of 2 nm HfSiON + 1 nm SiO2, buried oxide thickness (t_{BOX}) of 145 nm and 10 nm gate electrode of TiN + 100 nm of polysilicon. The method was tested for two devices, both with W_{fin} = 0.15 µm, one with L = 0.25 µm, and another with L = 1 µm.

IV. Results and Analysis

Initially, Fig. 4 and Fig. 5 were obtained from measurements performed on the shorter transistor. Fig. 4 represents the variation of the drain current as a function of the gate voltage at different external temperatures, while Fig. 5 represents the curves of drain current as a function of drain voltage for different V_{GS} values, varying with steps of 10mV, at room temperature. It should be noted that, to obtain a constant V_{GT} as was used later during the method, the V_t variation with the temperature must be taken into consideration.

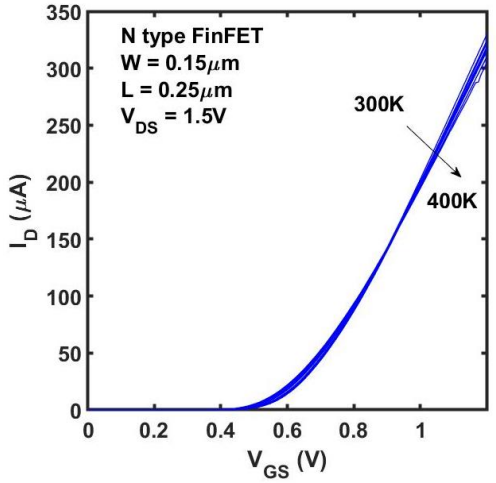

Fig. 4. Drain current as a function of gate voltage obtained through measurements performed in laboratory.

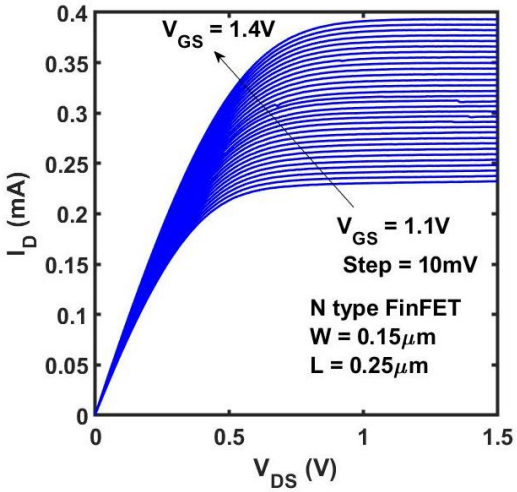

Fig. 5. Drain current as a function of drain voltage for different values of gate voltage.

The square root of I_D versus V_{GS} curves as a function of the external temperatures, which can be observed in Fig. 6, were used to extract V_t from 300 K up to 400 K, where the dashed lines represent the extension of the linear region of the square root of I_D. Then, for the first estimation of the c-factor, the g_m measurements were used for different values of T_{EXT}, as seen in Fig. 7, where the red markings represent the points of the same V_{GT}, considering the temperature variation of V_t.

Subsequently, the constant M is acquired from a linear approximation in the saturation region of the inverse transistor efficiency versus applied power, represented by the green line in Fig. 5, resulting in a value of M equal to 0.39 for the shorter transistor.

Finally, after the recursive process to better adjust the values and satisfy to the pre-established error condition, we obtained as a result the R_{TH} values shown in Table 1.

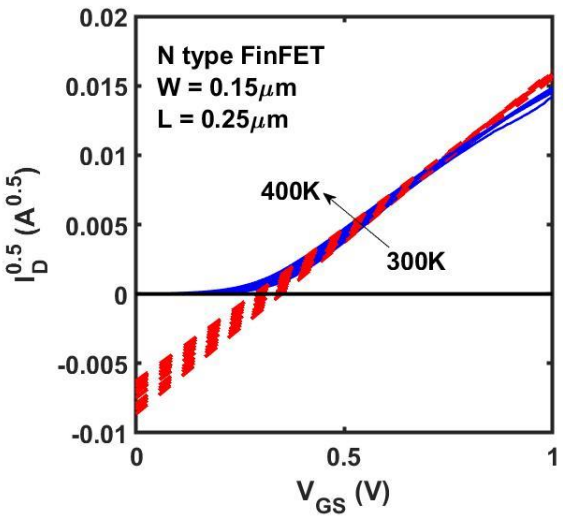

Fig. 6. Drain current as a function of gate voltage at different temperatures, where the dashed lines represent the extension of the linear region of the square root of drain current.

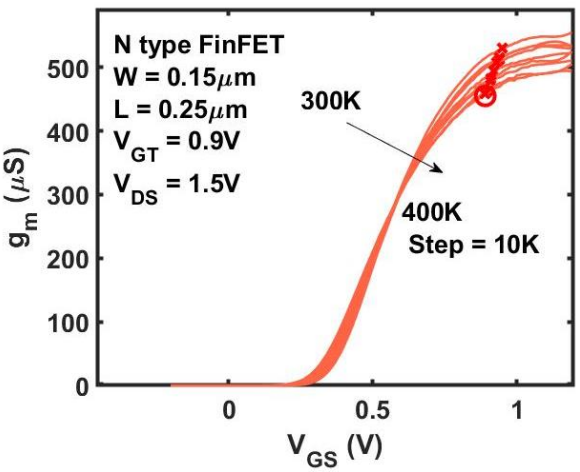

Fig. 7. Transconductance as a function of gate voltage at different temperatures, where the X markers represent the points with same V_{GT}.

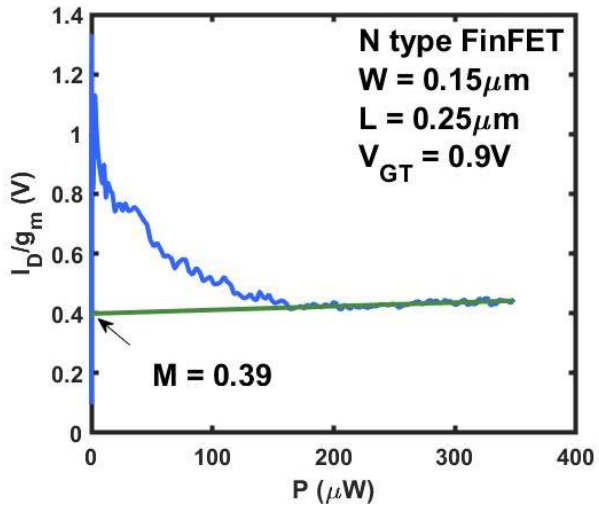

Fig. 8. The inverse transistor efficiency as a function of the power applied to the FinFET transistor.

TABLE I. THERMAL RESISTANCE IN FUNCTION OF THE CHANNEL LENGTH

Channel length (μm)	Thermal resistance (K/W)
0.25	$1.38*10^5$
1	$3.13*10^4$

The thermal resistance of these two different devices obtained through the algorithm used in the development of this work can be observed in Table I. It is verified that, the longer the channel length, the lower its thermal resistance, thus adding more evidence that reinforces the validity of the method, since, as shown in [5], devices with larger area have lower thermal resistance. Therefore, from the measurements performed for these devices, the algorithm used seems reliable to estimate the overall SHE behavior in advanced transistors.

V. CONCLUSION

In this work it was studied and reviewed the DC method for estimation of thermal resistance. The method applied in this paper is the only one that uses simple DC drain currents for estimation of thermal resistance, and it was successfully applied in FinFET devices with different channel lengths. From conventional current versus voltage curves, it was possible to estimate the thermal resistance by means of a recursive process, obtaining results that are in line with what was expected in the literature, but in an easier way.

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